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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of)	Art Unit: 2813
Hisashi OHTANI et al.)	Examiner: L. Schillinger
Serial No. 09/226,216)	CERTIFICATE OF MAILING
Filed: January 7, 1999)	I hereby certify that this correspondence is being deposited with
For: SEMICONDUCTOR DEVICE)	The United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents,
AND METHOD OF)	P.O. Box 1450, Alexandria, VA 22313-1450, on _/2-1.03
MANUFACTURING THE SAME)	- CC

RESPONSE

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

The Official Action mailed July 29, 2003, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to November 29, 2003. Accordingly, the Applicants respectfully submit that this response is being timely filed.

The Applicants note with appreciation the consideration of the Information Disclosure Statements filed on June 9, 2000, and May 2, 2002. The Applicants note again that the Information Disclosure Statement filed March 2, 1999, has not been acknowledged. As a courtesy, the Applicants have attached a copy of the Form PTO-1449 submitted March 2, 1999. The Applicants respectfully request that the Examiner provide an initialed copy of Form PTO-1449 evidencing consideration of the Information Disclosure Statement filed March 2, 1999.

Claims 5-9, 16-18, 20-22, 24-38 and 40-44 are pending in the present application, of which claims 5, 7, 16, 20 and 40-43 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action rejects claims 5-9, 16-18, 20-22, 24-38 and 40-44 as anticipated by U.S. Patent No. 6,087,679 to Yamazaki et al. The Applicants

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respectfully traverse the rejection because the Official Action has not established an anticipation rejection.

As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. <u>Verdegaal Bros. v. Union Oil Co. of California</u>, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

The Applicants respectfully submit that an anticipation rejection cannot be maintained against the independent claims of the present invention. Yamazaki does not teach all the elements of the independent claims, either explicitly or inherently.

It appears that Yamazaki discloses the steps of forming amorphous silicon film 503 over a substrate 501, crystallizing the amorphous silicon film 503 by a heat treatment with a catalyst element, patterning the crystallized silicon film to form an island-like semiconductor layer 508, forming a gate insulating film 509, removing or reducing the catalyst element, forming a gate electrode 513, adding an impurity element, and irradiating a laser to activate the impurity element (see columns 4-7 and Fig. 5 and 6).

Independent claims 5, 16, 40 and 41 of the present invention recite the steps of forming a gate electrode over an insulating surface, and forming a gate insulating film over the gate electrode. Yamazaki appears to teach forming a gate insulating film 509 and then forming a gate electrode 510 over the gate insulating film 509. Yamazaki does not teach, either explicitly or inherently, forming gate insulating film 509 over gate electrode 510. Therefore, the Applicants respectfully submit that Yamazaki does not teach forming a gate electrode over an insulating surface, and forming a gate insulating film over the gate electrode, either explicitly or inherently.

Further, independent claims 7 and 42 recite the steps of promoting crystallinity by irradiation of laser light or intense light and adding an impurity to said semiconductor film to form a pair of impurity regions in said semiconductor film after promoting crystallinity by irradiation of laser light or intense light. The Official Action asserts that "the laser annealing taught in Col. 7, lines: 45-50 [of Yamazaki] is to repair crystalline structure after implanting impurities into the active region" (page 11, Paper No. 30). In other words, the laser annealing in Yamazaki is performed after implanting impurities.

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The Yamazaki step of laser annealing after implanting impurities is not explicitly or inherently the same as adding an impurity after promoting crystallinity by irradiation of laser light or intense light. Therefore, the Applicants respectfully submit that Yamazaki does not teach promoting crystallinity by irradiation of laser light or intense light and adding an impurity to said semiconductor film to form a pair of impurity regions in said semiconductor film after promoting crystallinity by irradiation of laser light or intense light, either explicitly or inherently.

Further, independent claim 20 recites the step of patterning the crystallized semiconductor film into at least one semiconductor island after removing the film comprising germanium. Yamazaki appears to teach a step of gettering a catalyst element after patterning a semiconductor film to form an island-like semiconductor layer 508. The Yamazaki step of gettering after patterning is not explicitly or inherently the same as patterning after removing a film comprising germanium. Therefore, the Applicants respectfully submit that Yamazaki does not teach patterning the crystallized semiconductor film into at least one semiconductor island after removing the film comprising germanium, either explicitly or inherently.

Further, independent claim 43 recites the step of patterning the crystallized semiconductor film into at least one semiconductor island after irradiation of laser or intense light. Yamazaki appears to teach a step of irradiating a laser after patterning a semiconductor film to form an island-like semiconductor layer 508. The Yamazaki step of irradiating a laser after patterning is not explicitly or inherently the same as patterning after irradiation of laser or intense light. Therefore, the Applicants respectfully submit that Yamazaki does not teach patterning the crystallized semiconductor film into at least one semiconductor island after irradiation of laser or intense light, either explicitly or inherently.

Since Yamazaki does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102(e) are in order and respectfully requested.

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Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, Virginia 20165 (571) 434-6789

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AF 28/3

TRANSMITTAL FORM Application Number 09/226,216
Filing Date January 7, 1999
First Named Inventor Hisashi OHTANI et al.
Group Art Unit 2813
Examiner Name L. Schillinger
Attorney Docket Number 0756-1921

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December 1, 2003

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☐ Applicant Claims small entity status. See 37 CFR 1.27.

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Filing Date	January 7, 1999				
First Named Inventor	Hisashi OHTANI et al.				
Examiner Name	L. Schillinger				
Group Art Unit	2813				
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Name (Print/Type)	Eri	c J. Robinson	Registration No. 38,285 Telephone (571) 434-6789				39			
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